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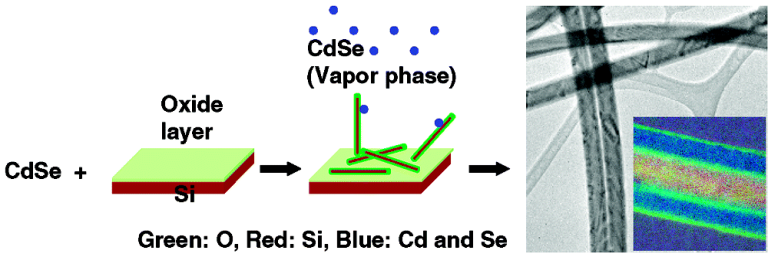


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# One-Step Fabrication of Uniform Si-Core/CdSe-Sheath Nanocables

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The integrated circuit industry has greatly inspired the fabrication of semiconductor heterostructures in two dimension, resulting in successful optoelectronic applications such as LEDs and laser diodes.[1] The formation of one-dimensional (1D) heterostructures is believed to be of the same importance in nanodevice fabrication.[2] Indeed, 1D heterostructures with modulated composition and interfaces have already demonstrated their potential in nanodevice applications with diverse functions.[3] Several groups have achieved 1D heterostructures based on different material systems, including semiconductor nanowire superlattices,[3,4] coaxial nanocables,[5,6] nanotypes,[7] and metal/insulator nanocables.[8,9]

As silicon is the most widely used material in the semiconductor industry, 1D silicon-based heterostructures on the nanometer scale are of general interest. It is known that single crystalline Si nanowires can be readily grown by various vapor transfer-based methods.[10−13] Using these Si nanowires as templates may result in various 1D Si-based heterostructures.[3,5] Nevertheless, multistep deposition involving change of the source material is usually troublesome. In this work, we design a simple one-step thermal evaporation of CdSe powder at controlled experimental conditions, which results in uniform Si-core/CdSe-sheath coaxial nanocables. Both the silicon core and the CdSe sheath are single crystalline. Oxygen is present at both the Si/CdSe interfaces and the outer surfaces of the nanocables.

Experimentally, an alumina tube was mounted horizontally inside a high-temperature furnace. The CdSe powder was placed in the center of the alumina tube. The tube was then pumped down to a base pressure of $2 \times 10^{-2}$ Torr. The furnace was heated 1200 °C for 2 h before it was cooled to room temperature. A constant flow of Ar was introduced at a flow rate of 50 sccm, and the total pressure in the tube was maintained at 300 Torr during the growth process. Silicon wafers were used as the substrates. They were first etched by 15% HF and then placed in the oxygen atmosphere for 2 h, which resulted in a thin oxide layer in the range of several nanometers. The substrates were located in the downstream of the tube.

The general morphology and chemical composition of the products were examined by secondary electron microscopy (SEM, LEO 1450VP) with an energy-dispersive X-ray (EDX, Oxford Instrument) spectrometer attached to the microscope. Figure 1a is a SEM image of the products collected from the silicon substrate. Uniform wirelike morphology is observed. The diameter of each individual wire is ≃80 nm, and the length is in the range of tens of micrometers. An EDX spectrum taken from the same sample is shown in Figure 1b, which indicates that the wires are composed of O, Si, Se, and Cd. The overall crystallinity of the product is examined by X-ray diffraction (XRD, Rigakau RU-300 with Cu $K\alpha_1$ radiation). All of the diffraction peaks can be indexed to cubic silicon and hexagonal CdSe within the experimental error.

Detailed microstructure analysis of the products was investigated by transmission electron microscopy (TEM) using a Tecnai 20 microscope (FEG, 200 kV). The elemental mapping was performed

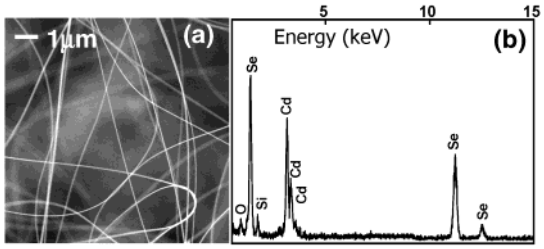


***Figure 1.*** (a) SEM image of the as-synthesized products, showing wirelike morphology; (b) EDX spectrum taken from the same sample, showing that they are composed of O, Si, Se, and Cd.

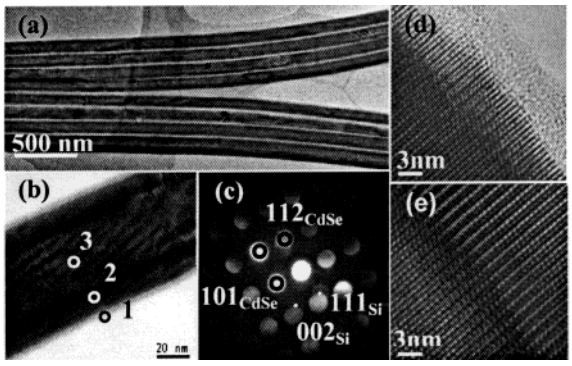


***Figure 2.*** (a) Low magnification TEM image showing uniform nanocables; (b) TEM image showing a single nanocable; (c) $\mu$-diffraction taken from the nanocable in (b), suggesting crystalline Si and CdSe; (d) high-resolution image showing the interface between areas 1 and 2 as marked in (b); (e) high-resolution image showing the interface between areas 2 and 3 as marked in (b). Both (d) and (e) were taken with electron beam along the CdSe [100] crystal direction.

using a Gatan image filtering (GIF) system attached to the same microscope. Figure 2a is a low magnification TEM image of several such wires. Light/dark contrast is observed in the corresponding core/sheath region of each individual nanowire. Such contrast is clearly demonstrated in Figure 2b, which is a higher magnification image of a single wire. The dark contrast suggests larger mass thickness in the sheath region. The Moiré fringes in the core region indicate the overlapping of crystals with different crystalline structures or orientations. A second sheath layer (light contrast), which is not obvious in Figure 2a, is observed outside the dark sheath region. These observations suggest that the "nanowire" is of a multisheath cable structure. Microdiffraction ($\mu$-diffraction) taken from the same wire shown in Figure 2b reveals two sets of diffraction spots (Figure 2c). One set of them can be indexed to those from hexagonal CdSe; others agree with the diffractions from cubic silicon. No specific orientation relation between the CdSe and the Si is suggested by the diffraction pattern. High-resolution images shown in Figure 2d and 2e were taken at the interfaces of regions 1 and 2, and regions 2 and 3 of the same wire, respectively (as marked in Figure 2b). A ≃5 nm thick amorphous layer, corresponding to region 1, is observed outside the single crystalline


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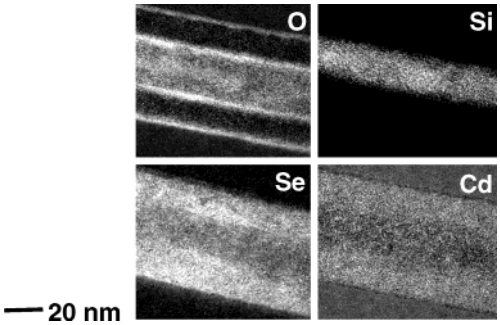


***Figure 3.*** Elemental maps of O, Si, Se, and Cd, taken at oxygen K edge (532 eV), silicon K edge (1839 eV), selenium L edge (1436 eV), and cadmium M edge (404 eV), respectively.

CdSe. Similar crystalline structures are observed in regions 2 and 3 (corresponding to hexagonal CdSe), with an interface not clearly resolved. The absence of Si lattice image further indicates the coaxial cable configuration (Si as the core) and the ill orientation relation between the CdSe and the Si.

The spatial distribution of different compositional elements is clarified by elemental mappings (Figure 3), which were performed using O K edge (532 eV), Si K edge (1839 eV), Se L edge (1436 eV), and Cd M edge (404 eV), respectively. Silicon and (Cd, Se) are located in the core and sheath region, respectively. This agrees well with the structural analysis shown in Figure 2. Oxygen content is high in two regions, that is, the outer surface of CdSe and the interface between CdSe and Si, indicating that both the CdSe and the silicon surface are oxidized. The region rich in oxygen is amorphous as no extra crystalline diffraction (both from X-ray and from electron diffraction) is detected.

The above results demonstrate that Si-core/CdSe-sheath nanocables are formed under the experimental conditions described above. Microdiffractions performed on several tens of such nanocables confirm the single crystallinity of both Si (cubic) and CdSe (hexagonal) in individual nanocables. The growth mechanisms of such nanostructures are discussed in the following.

The growth of the nanocable can be divided into two stages. In the first stage, silicon nanowires were formed on the silicon substrate via an oxide-assisted mechanism,[11−13] where silicon oxide plays important roles including serving as reactant in the disproportionation reaction[11,12] and terminating specific Si surfaces and thus inducing the anisotropic nanowire growth.[13] This is supported by several experimental facts: (1) No extra silicon source is provided, and no catalyst material is employed. (2) The nanocables (with Si core) are only found on the silicon substrate, indicating the Si substrate is the Si source. (3) The native oxide layer is important in forming the nanocables; freshly etched Si wafer (by HF) without exposure treatment in the $O_2$ atmosphere leads to a very low yield of such nanocables, which is qualitatively consistent with the $SiO_x$/Si ratio requirement for the Si nanowire growth.[11,12] (4) The nanocables are only formed at a specific temperature zone (∼900 °C) in the alumina tube, which agrees with the SiO decomposition temperature.[11,12] (5) A 5−10 nm oxide layer is present outside the silicon core (Figure 3, oxygen map) in the nanocable.

The CdSe starts to sublime at ∼1100 °C under the current experimental settings and is carried by the Ar to a lower temperature zone, where it condenses. In the second stage, the silicon nanowires lead to significantly increased surface area, which serves as the preferable adsorption site for the CdSe in the vapor phase and eventually works as the template for the one-dimensional growth of CdSe, resulting in the Si-core/CdSe-sheath nanocable heterostructures. Nevertheless, temperature >1200 °C only leads to large CdSe crystal growth due to the high supersaturation.[14] The isotropic nature of the amorphous oxide layer between the Si and the CdSe prevents the formation of any specific orientation relation between the two. The CdSe in the nanocables grow along a universal direction (CdSe [002]), which may be governed by thermodynamic/kinetic issues.[15] Our experiments show that thermal evaporation of CdSe under similar conditions but in the absence of Si substrate only results in CdSe nanorods (on the alumina tube wall) with universal growth direction along its [002] direction, further supporting the silicon nanowire templating argument. The outer surface oxide layer may be formed after the nanocables are exposed to air, as CdSe is known to be easily oxidized.[16]

In conclusion, Si-core/CdSe-sheath coaxial nanocables are fabricated via a simple one-step thermal evaporation process. The silicon nanowires can be directly grown from the silicon substrate via an oxide-assisted mechanism in the absence of extra Si source in the vapor phase and further serve as templates for the CdSe growth, resulting in nanocable heterostructures. Both the Si and the CdSe surfaces are oxidized, which constitutes a semiconductor(s)/insulator multisheath nanocable configuration. The oxide-assisted method results in fairly uniform silicon nanowires,[11] which leads to the narrow size distribution of the nanocables. This method can be applied to a wide range of materials and results in various Si-cored heterostructures, which may serve as potential building blocks in various nanodevices.

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**Supporting Information Available:** Description of the experimental results at different processing temperatures; XRD data of the as-synthesized nanocables; EEL spectra revealing the compositional elements of the nanocables and their chemical states; growth conditions of the pure CdSe nanorods (in the absence of Si substrate); SEM and TEM images of these CdSe nanorods (PDF). This material is available free of charge via the Internet at http://pubs.acs.org.

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